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Low Power, Accurate Variable-Gain Amplifier (VGA) with High dB-Linear Gain at 900MHz

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Abstract— *A 3-stage voltage controlled variable gain amplifier (VGA) for GHz range of application has been designed by using charge steering technique and simulated in a 65nm CMOS technology. The proposed voltage controlled VGA is characterized by wide range of gain variation, less temperature dependence gain characteristic, ultra-low power dissipation, low noise spectral density, small size, and voltage controllable dynamic gain range. It can be further used to design Voltage controlled oscillator, low power RF amplifiers, low power ADCs and other high frequency-low power CMOS circuits. The proposed voltage controlled VGA circuit is simulated in Tanner environment at 1.0V supply and 1GHZ clock frequency with 65nm CMOS technology. The result shows that the variable gain is in the range of− 20dB to +61dB with 3-dB gain bandwidth of 900MHz and power dissipation of 0.38mW.*

Keywords*: Charge Steering Technique (CST); Ultra Low Power (ULP); Voltage-Controlled Variable-Gain Amplifier (VC-VGA); Noise Spectral Density (NSD); dB-Linear Gain.*

1. INTRODUCTION

At the high frequency applications, variable gain amplifier (VGA) is found in many application, such as: telecommunication devices, medical equipment's, high frequency military application, disk drives, and others [1]-[3]. The VGA for these applications requires more than 30 dB of gain variation range. However, the 900MHz of band popularly has taken many applications in communication and microwave system [1]. The VGA is normally connected through a feedback loop to design an automatic gain control amplifier in communication systems. Therefore it is necessary to design a controlled VGA, which gain must be controlled by varying such parameter like voltage.

Previously proposed analog VGA, with the signal-multiplying technique using the Gilbert cell is discussed in [6]–[8], which offer low noise, low distortion, and high-frequency operation. However, the range of varying gain is limited to less than 20 dB, and the linearity error is significant [4]-[5]. To achieve a wide exponential gain variation by using bipolar transistors is an effective solution [6], but this requires very high power dissipation and is not compatible with standard CMOS technology [7]. The VGAs also can be implemented with BiCMOS technology, but it is not an effective solution in term of cost [4].

However, charge steering technique (CST) is the transformation of continuous time topology into the discrete time topology by using switches and capacitors [11]. Therefore, CST plays a major role to reduce power dissipation of amplifiers, which is further used to design mixed analog-digital CMOS circuits. The transformation of charge steer from current steer on differential pair is shown in Fig.1 [11].

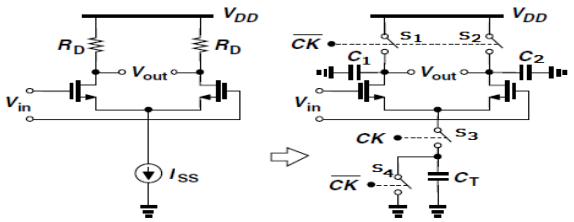

Fig. 1: Transformation of charge steering from current steering.

The operation of CST in Fig.1 depends on clock (CK) and is in two modes: reset mode and amplification mode. In Reset mode, CK goes low, switches S_1, S_2 and S_4 are ON and S_3 is OFF. C_1 and C_2 charged to V_{DD} and C_T discharged to GND. When CK goes high, S_3 is ON, C_T pulls current through MOSFETs and output nodes release and circuit operates in amplification mode.

In this paper, we proposed an efficient design to boost gain and to reduce power dissipation of VC-VGA by using the concept of CST. The rest of the paper structured as: Section II contains proposed circuit and analysis of different parameters. Section III discusses modified design to reduce noise spectral density (NSD) and temperature effect. Section IV contains simulation result and discussion followed by Section V as conclusion.

2. PROPOSED DESIGN

In this section we have introduced the proposed design of voltage controlled VGA and the gain analysis which is used to design 3-stage VGA.

3. BASIC IDEA

By transforming the continuous behavior into discrete time, Fig. 2 shows the proposed VC-VGA. By comparing with conventional typologies [4]-[10] , this design exhibits pure transistor topology, In which R_D is changed by PMOS (M7 and M8), Between V_{DD} and output node, and capacitor, between output node and GND. I_{SS} is transformed as shown in Fig. 2, using transistors M9, M10 and Capacitor C_T. To control the behavior of MOSFETs (M7, M8, M9, M10) as a switch, the gate of these MOSFETs connected with clock CK. This circuit operates in Reset mode (CK low) and in Amplification mode (CK high). When CK goes low, M7, M8 and M9 are ON and in saturation. Therefore, C_1 and C_2 charge at bellow one threshold of supply voltage (i.e. V_{DD}-$V_{THP,7}$) and C_T discharges through on resistance r_O of M10. In Reset mode if we consider the charging time of capacitor C_1 as $\tau_{charging,C1}$, then

$$\tau_{charging,C1} = r_{O,7}\, C_1 \quad (1)$$

Similarly for C_2,

$$\tau_{charging,C2} = r_{O,8}\, C_2 \quad (2)$$

Thus, the selection of C_1 and C_2 such that the $\tau_{charging,C1} << T_{CK}$. Similarly, we can conclude the selection of C_T as depending on charging and discharging time.

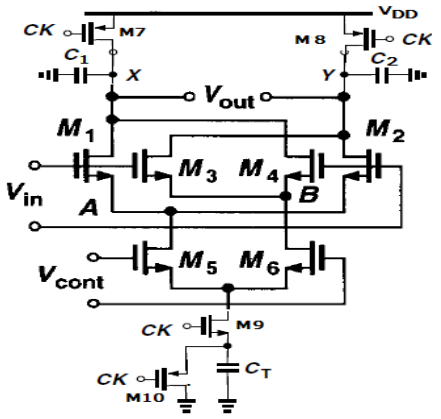

Fig. 2: Proposed VC-VGA circuit

When CK goes high, M9 is ON and in saturation and circuit enters in Amplification mode. Now, the V_{cont} which is applied through M5 and M6, controls the circuit operation in amplification mode. If V_{cont} is (+)ve, M1 and M2 will ON and $V_{out} = g_{m5,6}\, r_O\, V_{in}$. Similarly if V_{cont} is (-)ve then M3 and M4 are ON and $V_{out} = -g_{m5,6}\, r_O\, V_{in}$. Therefore, it is seen very clearly that current steer does not affect the conventional operations of VC-VGA.

The proposed VC-VGA circuit also exhibits the functionality as analog voltage multiplier. It is because of the gain of the circuit is function of $V_{cont} = V_{cont1}$-V_{cont2}, therefore we have $V_{out} = V_{in}$. $f(V_{cont})$. With Taylor expansion of $f(V_{cont})$, and neglecting higher order terms, we have $V_{out} = \alpha\, V_{in}$. V_{cont}. In general this property of voltage multiplying is exhibits in any VGA which are controlled by voltage.

Gain Analysis: To analysis the gain of proposed single stage VGA circuit, let us consider the output behavior dependency at V_{cont}. If V_{cont} is (+)ve, M1 and M2 will ON and $V_{out} = g_{m5,6}\, r_O\, V_{in}$. Similarly if V_{cont} is (-)ve then M3 and M4 are ON and $V_{out} = -g_{m5,6}\, r_O\, V_{in}$. Therefore the gain,

$$A_v = A_{v1}[V_{cont}=+ve] + A_{v2}[V_{cont}=-ve] \quad (3)$$

Now putting the value of A_{v1} and A_{v2}, we get

$$A_{v1}[V_{cont}=+ve] = -\mu C_{OX}(W/L)_{5,6}\,(V_{gs5,6} - V_{th5,6})\, r_{o1,2} \quad (4)$$

$$A_{v1}[V_{cont}=-ve] = -\mu C_{OX}(W/L)_{5,6}\,(V_{gs5,6} - V_{th5,6})\, r_{o3,4} \quad (5)$$

From (4) and (5), $V_{gs5,6} - V_{th5,6} = V_{cont} - V_{DS5,6} - V_{th5,6}$, therefore, it is shown that the gain can be control through (W/L) ratio, V_{cont}, $V_{th5,6}$ and $r_{o(1,2,3,4)}$. It implies that for high gain, $(W/L)_{5,6}$ and V_{cont} should be high.

The output impedance r_o can be scaled also by changing the channel length L, as channel modulation factor 'λ' is inversely proportional to 'L' and hence r_o becomes the factor of 'L/I_D' (as $r_o = 1/\lambda I_D$). Therefore a longer transistor yields a higher voltage gain.

4. GAIN BOOSTING BY STAGE CASCADING

This section is introduced the cascading at the 3-stage to boost the gain by using proposed VGA design.

To more efficient design toward the gain boosting and noise with DC offset reducing, the cascade structure of [6] is used and modified as shown in Fig.3 up to 3-stage. VGA1, VGA2 and VGA3 are the proposed VC-VGA circuits of Fig.2. VGA1 and VGA 2 are designed with 32.5dB (− 10 to 21.5) gain control range with 6.5dB step for coarse tuning and VGA3 is designed with 16dB (0 to 16dB) gain control range with 2dB step for fine tuning. Therefore this design is provided high tunable range only in 3-stage.

The architecture design of Fig.3 is also able to reduce the noise effect by reducing noise spectral density (NSD) at the low frequencies. As the noise becomes more effective at low frequency because of '1/f' flicker noise effect. To reduce the NSD (input referred noise) at low frequency, a high pass filter (HPF) is added at input node. Therefore applied noise at low frequencies is rejected by HPF and only high frequencies noise is passed, which are negligible.

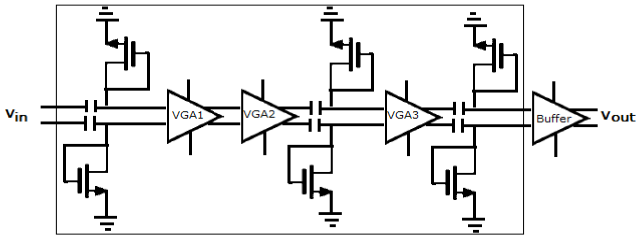

Fig. 3: Architecture of 3-stage VGA using proposed VC-VGA circuit

To design a high pass filter, the transistors are used and operated in saturation. Therefore, an equivalent resistance $r_{on,N}$ is drawn, which reduces the VGA active area. The 3-stage VGA increases settling time and dynamic power but also increases gain and reduces sufficient amount of noise spectral density ie, noise at very low frequency. This design is also eliminated the DC offset due to self-mixing which are produced at preceding stages. At output node, a buffer is employed for testing purposes.

The gain of 3-stage cascaded VGA is calculated as,

$$A_{v,tot} = A_{v,VGA1} \cdot A_{v,VGA2} \cdot A_{v,VGA3} \quad (6)$$

As we designed VGA1 and VGA2 symmetrically, then the gain of VGA1 and VGA2 are equal. Therefore,

$$A_{v,tot} = (A_{v1} + A_{v2})^2_{VGA1,2} \cdot (A_{v1} + A_{v2})_{VGA3}$$

5. SIMULATION RESULT AND DISCUSSION

In this section we are discussed about the simulation results and parameter selection framework, such as (W/L) ratio and V_{th} of each MOSFET's to control the gain at each stage. All the results are simulated in Tanner environment with 65nm CMOS technology at VDD=1.0V, Temp = 25^0C, F_{CK} = 1GHz. The rest of the design specification discussed as follow:

Fig.4 shows the transient analysis of proposed single stage VGA. In the transient analysis the control voltage is ramp signal varied from -2 to 2 Volt and the input voltage is applied as sinusoidal of 200MHz frequency. The clock frequency is a square wave of 0.5ns period with 50ps of rise and fall time. Therefore, the F_{CK} is 1GHz. The variation of output waveform follow the sinusoidal waveform with DC offset shift depending on V_{cont}. The peak to peak output voltage swing is $600mV_{pp}$.

Because of the greater dependencies of the voltage gain of proposed VGA on (W/L) ratio and V_{th}, this is important to design each stage with demanding gain. For VGA1 and VGA2 stages, the variable gain range is− 10dB~21.5dB thus it is designed with large (W/L) ratio and high V_{th}. At given r_o, in the range of 10's of Kilo ohms, the g_m should be in the range of 10's of µA/V to the range of mA/V. Therefore the (W/L) of transistors in VGA1 and VGA2 are selected as $(200/0.25)_{(1,2,3,4)}$, $(20/0.25)_{(5,6,9)}$ and $(30/0.25)_{(7,8,10)}$. Similarly, for VGA3 stage, the variable gain range is 0~16dB and it is designed with small (W/L) ratio and low V_{th}. Therefore, by selecting appropriate parameter, the gain is controlled by V_{cont}.

Fig.5 shows the dB-linear Voltage gain variation plot verses control voltage varying from 0.2 to 1.2V. The graph shows that the voltage gain is highly linear. The total varying dB-linear range is 32.5dB (VGA1 and VGA2) and 16dB (VGA3), and for VGA1 and VGA2 stages the variable gain level is 5dB and for VGA3 is 8dB. Therefore the step increment is 6.5dB and 2dB respectively.

Fig.6 shows the voltage gain plot for VGA3 by varying frequency in dB scale at different control voltage. The gain is allowed to vary from 0 to 16dB at 8 gain level as V_{cont} varies from 0.2 to 1.2V respectively. The 8 gain levels are selected for the purpose of fine tuning range at VGA3 stage. Therefore, we selected the step increment only by 2dB.

Table I shows the performance comparison of VGA designed at each stage. VGA3 consumed less power comparison of VGA1 and 2 but more leakage current. Each stage provides input referred noise (NSD) of $10.23nV/Hz^{1/2}$. The voltage swing for VGA1&2 are $600mV_{pp}$ and for VGA3 is $410mV_{pp}$.

Fig.7 shows the Bode plot of loop gain for proposed VGA3 at different temperature. The gain bandwidth of the VGA3 at room temerature is 900MHz. The proposed VGA3 design gives(Tess variation in gain with temperature. As gain varies from 6dB to 25dB as temperature varies from−40^OC to 100^OC with step=20^OC.

Table II. shows the performance comparison of 3-stage VGA with privious work done [4]-[10]. The dB-Linear gain is 81dB

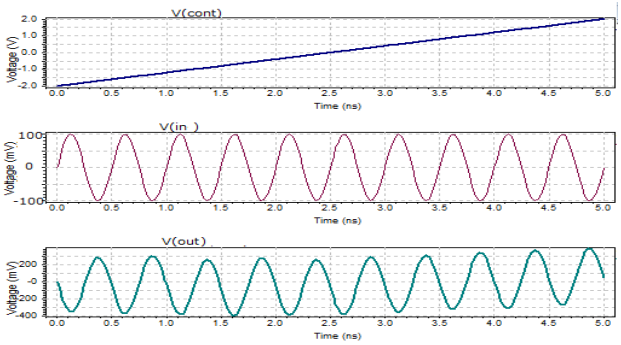

Fig. 4: Transient responce of proposed VGA circuit at F_{CK}=1GHz

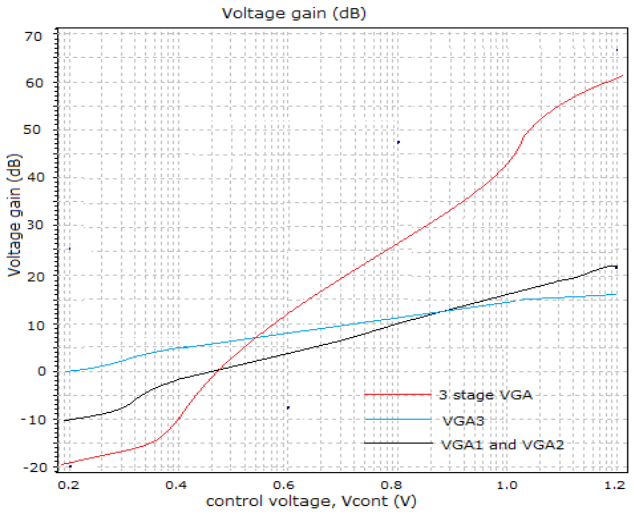

Fig. 5: dB-linear Voltage gain variation plot verses control voltage

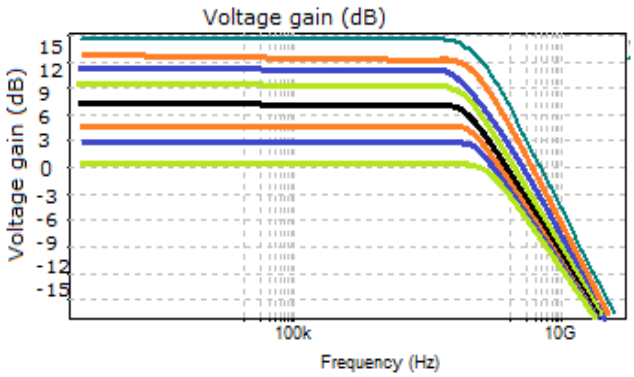

Fig. 6: Voltage gain at 8 gain level for VGA3 circuit for fine tuning

in the range of -20dB to 61dB (gain error is ±0.58dB). In Table II, it is shown that the 3dB bandwidth of 3-stage VGA is 900MHz. The VGA with 900MHz frequency is applicable in many RF receivers. The 3-stage VGA dissipates only 0.38mW of power at 1.0V supply and the total area is 0.021mm^2. The power is reduced because of CST applied and area is reduced because of pure transistor topology. At the supply of 1.0V, the output swing is found to be 0.6V$_{pp}$ and input referred noise

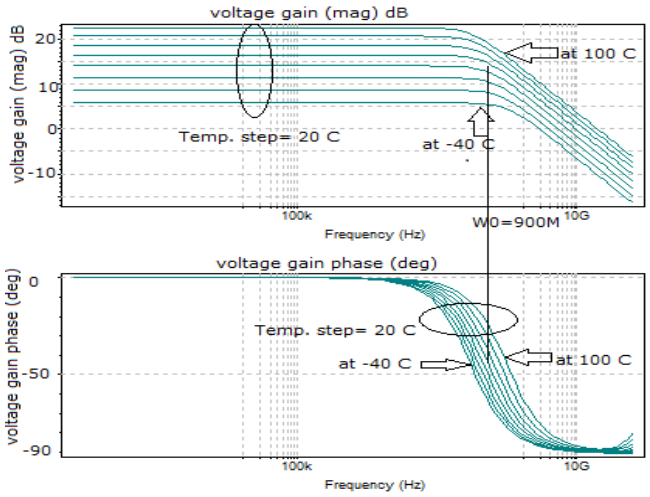

Fig. 7: Bode plot of voltage gain for proposed VGA3 at different temperature (-40^{0}C to 100^{0}C with step=20^{0}C)

Table 1: Performance of Proposed VGA

	VGA1 and VGA2a	VGA3a
Gain range (dB)	−10 ~ 21.5	0 ~ 16
dB- linear range (dB)	32.5	16
Gain level (dB)	5	8
Step increment (dB)	6.5	2
Power (µW)	14.62	9.68
Leakage current (nA)	1.59	2.77
NSD (nV/Hz1/2)	10.23	10.23
Output swing (Vpp)	0.6	0.41

Table 2: Performance comparison of 3-stage VGA

	[4]	[5]	[6]	[7]	[8]	[9]	[10]	This work
#Stages	2	3	3	3	2	3	4	3
Gain variation (dB)	-52 to 43	-15 to 60	-13 to 63	6 to 21	-30 to 20	-12 to 21	-39 to 20.2	-20 to 61
dB- linear range (dB)	95	75	50	15	50	33	60	81
Bandwidth (Hz)	1.05G	270M	14.8 M	1.2 G	1.2 G	20 G	4G	900 M
NSD (nV/Hz1/2)	(*)	(*)	3.5	(*)	(*)	(*)	(*)	5.63
Supply (V)	1.8	1.8	1.2	1.2	1.2	1.2	1.2	1.0
Power (mW)	6.5	11.8	3.84	7.5	1.4	10.9	26	0.38
Swing (Vpp)	(*)	(*)	(*)	0.5	0.4	(*)	(*)	0.6
Area (mm2)	0.4	0.06	0.01	0.3	(*)	0.25	0.06	0.021
Technology (CMOS)	0.18µm	0.18µm	65 nm	65 nm	65 nm	65 nm	65 nm	65nm
Gain control	A	D	D	D	D	D	A	D

(*) Not reported, A=analog, D=digital

(NSD) is 5.63nV/Hz$^{1/2}$. The NSD is reduced because of HPF in 3-stage VGA.

6. CONCLUSION

The digitally controlled 3-stage VGA is proposed for low power-high gain, based on Charge Steering Technique, and realized in 65nm CMOS technology. The proposed design reduces area and power dissipation at 1GHz clock frequency. It is designed to operate at high frequencies range in GHz. The tunable 81dB-linear gain range within ±0.58dB gain error, varying from−20dB to 61dB at 900MHz of 3dB bandwidth is achieved. The proposed VGA dissipates an average power of 0.38mW from 1.0V supply.

7. ACKNOWLEDGMENT

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